AF/2823

Image

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Before the Board of Patent Appeals and Interferences

In re Patent Application of
ONISHI
Serial No. 09/834,923
Filed: April 16, 2001

Atty Dkt. 925-190
C# M#
TC/A.U.: 2823
Examiner: Maldonado, J.
Date: February 23, 2004

OIPE FEB 23 2004 PATENT & TRADEMARK OFFICE

Title: SEMICONDUCTOR DEVICE PRODUCING METHOD AND SEMICONDUCTOR DEVICE

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

☐ **Correspondence Address Indication Form Attached.**

☐ **NOTICE OF APPEAL**
Applicant hereby **appeals** to the Board of Patent Appeals and Interferences from the last decision of the Examiner. ($ 330.00) $

☒ An appeal **BRIEF** is attached in triplicate in the pending appeal of the above-identified application ($ 330.00) $ 330.00

☐ Credit for fees paid in prior appeal without decision on merits -$ ( )

☐ A reply brief is attached in triplicate under Rule 193(b) **(no fee)**

☐ Petition is hereby made to extend the current due date so as to cover the filing date of this paper and attachment(s) **($110.00/1 month**; $420.00/2 months; **$950.00/3 months**; $1480.00/4 months) $

SUBTOTAL $ 330.00

☐ Applicant claims "Small entity" status, enter ½ of subtotal and subtract -$( )
☐ "Small entity" statement attached.

SUBTOTAL $ 330.00

Less month extension previously paid on -$(0.00)

TOTAL FEE ENCLOSED $ 330.00

Any future submission requiring an extension of time is hereby stated to include a petition for such time extension. The Commissioner is hereby authorized to charge any deficiency, or credit any overpayment, in the fee(s) filed, or asserted to be filed, or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our **Account No. 14-1140.** A duplicate copy of this sheet is attached.

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NIXON & VANDERHYE P.C.
By Atty: Joseph A. Rhoa, Reg. No. 37,515

Signature: _____

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Patent Application of

ONISHI — Atty. Ref.: 925-190

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* *

February 23, 2004

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APPEAL BRIEF

Sir:

Applicant hereby **appeals** to the Board of Patent Appeals and Interferences from the last decision of the Examiner.

REAL PARTY IN INTEREST

The real party in interest is Sharp Kabushiki Kaisha, a corporation of the country of Japan.

RELATED APPEALS AND INTERFERENCES

The appellant, the undersigned, and the assignee are not aware of any related appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

STATUS OF CLAIMS

Claims 1-7 and 9-12 are pending and have been rejected. No claims have been substantively allowed.

STATUS OF AMENDMENTS

No amendments have been filed since the date of the Final Rejection. However, the Response After Final filed November 5, 2003 has been entered and considered by the Examiner as indicated in the Advisory Action dated November 24, 2003.

SUMMARY OF EXAMPLES OF INVENTION

For purposes of example, and without limitation, certain example embodiments of this invention relate to a method of making a semiconductor device.

For example, Fig. 1 of the instant application illustrates a substrate 1 which supports interlayer insulator layer 2 and barrier film 3. A contact hole formed in interlayer insulator layer 2 and barrier film 3 is then filled with a plug (4 and/or 5). Thereafter, insulation film 6 and adhesion film 11 are formed over the plug and barrier.

In the example Fig. 1 embodiment, insulation film 6 and then adhesion film 11 are formed on the plug (4 and/or 5) and the barrier film 3. Then, hole 6a is formed in both the insulation film 6 and the adhesion film 11 leading to the plug 4/5 such that an upper surface of the plug and an adjacent part of the barrier film 3 are exposed. In other words, ***insulation film 6 and adhesion film 11 are formed before forming a hole therein.*** Thereafter, a first conductive film 7 is formed on the insulation and adhesion films 6 and 11, respectively, and on and over an exposed part of the barrier film 3 in the hole 6a such

that the hole 6a in the insulation film and in the adhesion film is filled with the first conductive film 7. Then, the conductive film 7 and adhesion film 11 are subject to CMP to form a lower electrode 8 within the hole in the insulation film. The ***adhesion film 11 is removed before the lower electrode is left in the protuberant manner*** as shown in Fig. 1D.

The adhesion film required by claim 1 is formed on the first insulation film in order to provide good adhesion between the insulation film and the first conductive film (e.g., to provide good adhesion between insulation film 6 and first conductive film 7 as shown in Fig. 1B of the instant application) (e.g., pg. 11, lines 6-12; pg. 15, lines 9-13; and pg. 20, lines 10-15). Generally speaking, the lower electrode material has poor adhesion to the insulation film. Therefore, without the claimed adhesion film set forth in claim 1, the first conductive film may become detached from the insulation film during the claimed CMP process thereby leading to product failure. Thus, it can be seen that providing the claimed adhesion film between the insulation film and the electrode, and then removing the same before the lower electrode is left in the protuberant manner as shown in Fig. 1D, solves a significant problem in the art and leads to a much improved product with better yields.

ISSUES

1. Whether claims 1-7 and 9-12 are unpatentable under 35 U.S.C. Section 103(a) over Hieda (US 6,335,241) in view of Zurcher (US 6,344,413).

GROUPING OF CLAIMS

The claims are divided into the following separate and distinct groups which are patentably distinct from one another:

Group A: Claims 1-3, 10 and 12.

Group B: Claims 4-9 and 11.

Thus, for example, claims 1-3, 10 and 12 stand/fall together. Moreover, as another example, claims 1 and 4 do not stand/fall together.

ARGUMENT

It is axiomatic that in order for a reference to anticipate a claim, it must disclose, teach or suggest each and every feature recited in the claim. See, e.g., Kalman v. Kimberly-Clark Corp., 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983). The USPTO has the burden in this respect.

Moreover, the USPTO has the burden under 35 U.S.C. Section 103 of establishing a *prima facie* case of obviousness. In re Piasecki, 745, F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). It can satisfy this burden only by showing that some objective teaching in the prior art, or that knowledge generally available to one of ordinary skill in the art, would have led that individual to combine the relevant teachings of the references to arrive at the claimed invention. In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). Before the USPTO may combine the disclosures of the references in order to establish a *prima facie* case of obviousness, there must be some suggestion for doing so. In re Jones, 958 F.2d 347 (Fed. Cir. 1992). Even assuming, *arguendo*, that a given combination of references is proper, the combination of

references must in any event disclose the features of the claimed invention in order to render it obvious.

Claim 1 (together with claims 2-3 and 10-12)

Claim 1 stands rejected under 35 U.S.C. Section 103(a) as being allegedly unpatentable over Hieda in view of Zurcher. This Section 103(a) rejection should be reversed for at least the following reasons.

Claim 1 requires ". . . . forming an insulation film and then an adhesion film on the plug and the barrier film, and ***then*** forming a hole in the insulation film and the adhesion film leading to the plug such that an upper surface of the plug and an adjacent part of the barrier film are exposed . . . . wherein the adhesion film is removed before the lower electrode is left in the protuberant manner; forming a dielectric film that covers the protuberant lower electrode and at least part of the barrier film, and then forming a second conductive film that covers at least part of the dielectric film, said dielectric film being made of a ferroelectric or high-dielectric-constant substance; and patterning the dielectric film and the second conductive film simultaneously to thereby form a capacitor dielectric film and an upper electrode."

For example, see Fig. 1 of the instant application which illustrates adhesion film 11. In the example Fig. 1 embodiment of the instant application, insulation film 6 and then adhesion film 11 are formed on the plug (4 and/or 5) and the barrier film 3. Then, hole 6a is formed in both the insulation film 6 and the adhesion film 11 leading to the plug 4/5 such that an upper surface of the plug and an adjacent part of the barrier film 3 are exposed. In other words, ***insulation film 6 and adhesion film 11 are formed before forming a hole therein***. Thereafter, a first conductive film 7 is formed on the insulation

and adhesion films 6 and 11, respectively, and on and over an exposed part of the barrier film 3 in the hole 6a such that the hole 6a in the insulation film and in the adhesion film is filled with the first conductive film 7. Then, the conductive film 7 and adhesion film 11 are subject to CMP to form a lower electrode 8 within the hole in the insulation film. The ***adhesion film 11 is removed before the lower electrode is left in the protuberant manner*** as shown in Fig. 1D.

The adhesion film required by claim 1 is formed on the first insulation film in order to provide good adhesion between the insulation film and the first conductive film (e.g., to provide good adhesion between insulation film 6 and first conductive film 7 as shown in Fig. 1B of the instant application) (e.g., pg. 11, lines 6-12; pg. 15, lines 9-13; and pg. 20, lines 10-15). Generally speaking, the lower electrode material has poor adhesion to the insulation film. Therefore, without the claimed adhesion film set forth in claim 1, the first conductive film may become detached from the insulation film during the claimed CMP process thereby leading to product failure. Thus, it can be seen that providing the claimed adhesion film between the insulation film and the electrode, and then removing the same before the lower electrode is left in the protuberant manner as shown in Fig. 1D, solves a significant problem in the art and leads to a much improved product with better yields.

The Office Action admits that Hieda fails to disclose or suggest the formation of the claimed adhesion film, let alone at the time required by claim 1 (e.g., pg. 4 of Office Action, first paragraph). Thus, the Examiner has *admitted* that Hieda fails to disclose or suggest the aforesaid underlined aspects of claim 1. Recognizing these flaws in Hieda, the Office Action cites Zurcher.

However, (1) Zurcher also fails to disclose or suggest forming an insulation film and an adhesion film thereon *before* forming a hole therein. Additionally, (2) Zurcher fails to disclose or suggest removing such as adhesion film before the lower electrode is left in a protuberant manner as required by claim 1. Thus, Zurcher fails to disclose or suggest each of theses two [(1) and (2)] aspects of claim 1. Thus even if the two references were combined as alleged in the final rejection (which applicant believes would be incorrect in any event due to a lack of suggestion/motivation), the invention of claim 1 still would not be met.

(1) Zurcher teaches that a Ti adhesion film may be formed just before forming barrier layer 208 (e.g., col. 6, lines 35-40; and Figs. 11-12). However, this means that Zurcher's non-illustrated Ti adhesion film would be formed *after* formation of the hole in insulator 206. In contrast, claim 1 requires that the adhesion film and insulation film be formed *before* the hole is formed in both the insulation film and the adhesion film.

Thus, it can be seen that both Hieda and Zurcher fail to disclose or suggest forming an adhesion film and insulation film *before* a hole is formed in both the insulation film and adhesion film as called for in claim 1. Accordingly, even if the two references were combined as alleged in the Office Action (which applicant believes would be incorrect in any event), the invention of claim 1 still would not be met.

In the Advisory Action, the Examiner argues that the non-illustrated Ti adhesion film referred to at col. 6, lines 35-40 of Zurcher would be formed on the top surface of layer 218 before the contact hole is formed in layer 218 because the purpose of the adhesion film is to improve adhesion between layers 218 and 208. First of all, it is noted that Zurcher does not disclose or suggest this. Moreover, Fig. 11 of Zurcher illustrates

that layer 208 is adhered to layer 218 not just on the top surface thereof, *but also on side surfaces thereof* in the contact hole. Thus, in order to improve adhesion between layers 208 and 218, *including at the sidewall portions*, the non-illustrated adhesion film must be formed *after* the contact hole is formed in layers 218, 206 – this is expressly excluded by claim 1. Accordingly, in view of the purpose for providing the adhesion film in Zurcher, this film must be formed after forming the contact hole in layers 218, 206. Thus, the Examiner's new argument that the adhesion film may be formed before the contact hole is formed in layers 206, 208 lacks merit and is unsupported by the cited art itself since the art fails to disclose or suggest this.

(2) Additionally, claim 1 requires that the adhesion film be "removed before the lower electrode is left in the protuberant manner." For example, it can be seen in Fig. 1 of the instant application that adhesion film 11 is removed (see Figs. 1B-1C) before the electrode 8 is left in a protuberant manner in Fig. 1D. In contrast, *Zurcher's Ti adhesion film is never removed.* Thus, Zurcher cannot possibly disclose or suggest removing the adhesion film before the lower electrode is left in the protuberant manner as required by claim 1. It is noted that Zurcher's leaving the adhesion film in place forever is problematic because potential oxiding of the adhesion layer may undesirably increase contact resistance.

Since both cited references fail to disclose or suggest the claimed removal of the adhesion film before the lower electrode is left in the protuberant manner, even the alleged combination fails to meet the invention of claim 1. The Section 103(a) rejection is fundamentally flawed for this additional reason.

In the Advisory Action, the Examiner appears to argue that it is theoretically possible that a small portion of the adhesion film in Zurcher may be removed for contact hole formation. First, applicant notes that Zurcher does not disclose or suggest this (the Examiner's allegation is based on impermissible hindsight and speculation). Second, it is important to note that claim 1 does not say that "part" of the adhesion film is removed as the Examiner tries to argue. The recitation in claim 1 of "the adhesion film" being removed necessarily refers to the entire adhesion film – not just part of it. Thus, claim 1 requires that the adhesion film (not just part of it) be removed before the lower electrode is left in the protuberant manner. For each of the aforesaid reasons, it can be seen that the cited art fails to disclose or suggest this, either taken alone or in the alleged combination.

For each of the aforesaid reasons (1) and (2), the Section 103(a) rejection of claim 1 is fundamentally flawed and should be reversed.

Claim 4 (together with claims 5-9 and 11)

Claim 4 also stands rejected under 35 U.S.C. Section 103(a) as being allegedly unpatentable over Hieda in view of Zurcher. This Section 103(a) rejection should be reversed for at least the following reasons.

Claim 4 requires "forming a first insulation film and then an adhesion film on the plug and the barrier film, and then forming a hole leading to the plug in the first insulation film and the adhesion film such that an upper surface of the plug is exposed . . . . . etching the second insulation film until an upper surface of the first conductive film is reached, and then etching the first conductive film, the adhesion film, and the second insulation film in the hole by a chemical mechanical polishing method until the first insulation film is exposed, to thereby form a cup-shaped lower electrode within the hole."

Thus, it can be seen that claim 4 requires (1) forming an insulation film and an adhesion film thereon *before* forming a hole therein, and (2) etching the first conductive film, adhesion film, and second insulation film in the hole by CMP until the first insulation film is exposed.

As explained above, the cited art fails to disclose or suggest these aspects of claim 4, either taken alone or in combination. The Office Action admits that Hieda fails to disclose or suggest these aspects of claim 4, and instead relies on Zurcher in these respects. However, as explained above, Zurcher fails to disclose or suggest each of these aspects of claim 4. Thus, even if the two references were combined as alleged in the Office Action (which applicant believes would be incorrect in any event), the invention of claim 4 still would not be met. The Section 103(a) rejection of claim 4 should be reversed..

CONCLUSION

In conclusion it is believed that the application is in clear condition for allowance; therefore, early reversal of the Final Rejection and passage of the subject application to issue are earnestly solicited.

Respectfully submitted,

NIXON & VANDERHYE P.C.

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APPENDIX

CLAIMS ON APPEAL

1. A method of producing a semiconductor device, the method comprising:

sequentially forming an interlayer insulating film and a barrier film on a semiconductor substrate;

making a contact hole in the barrier film and the interlayer insulating film, and forming a plug within the contact hole;

forming an insulation film and then an adhesion film on the plug and the barrier film, and then forming a hole in the insulation film and the adhesion film leading to the plug such that an upper surface of the plug and an adjacent part of the barrier film are exposed;

forming a first conductive film on the insulation and adhesion films and on and over an exposed part of the barrier film in the hole such that the hole in the insulation film and in the adhesion film is filled with the first conductive film, and then etching the first conductive film and the adhesion film by a chemical mechanical polishing method to thereby form a lower electrode within the hole in the insulation film;

etching the insulation film until the barrier film is exposed, so as to leave the lower electrode in a protuberant manner;

wherein the adhesion film is removed before the lower electrode is left in the protuberant manner;

forming a dielectric film that covers the protuberant lower electrode and at least part of the barrier film, and then forming a second conductive film that covers at least

part of the dielectric film, said dielectric film being made of a ferroelectric or high-dielectric-constant substance; and

patterning the dielectric film and the second conductive film simultaneously to thereby form a capacitor dielectric film and an upper electrode.

2. The method according to claim 1, wherein said barrier film is made of TiO_2 or Al_2O_3 or SiN.

3. The method according to claim 1, wherein said adhesion film comprises a Ti film or a TiO_2 film on the insulation film.

4. A method of producing a semiconductor device, the method comprising:

sequentially forming an interlayer insulating film and a barrier film so as to be supported by a semiconductor substrate;

making a contact hole in the barrier film and the interlayer insulating film and forming a plug within the contact hole;

forming a first insulation film and then an adhesion film on the plug and the barrier film, and then forming a hole leading to the plug in the first insulation film and the adhesion film such that an upper surface of the plug is exposed;

forming a first conductive film over at least part of the first insulation film and adhesion film and within the hole such that the first conductive film within the hole does not fill the hole but covers surfaces defining the hole, and then forming a second insulation film on the first conductive film so as to fill the hole;

etching the second insulation film until an upper surface of the first conductive film is reached, and then etching the first conductive film, the adhesion film, and the second insulation film in the hole by a chemical mechanical polishing method until the first insulation film is exposed, to thereby form a cup-shaped lower electrode within the hole;

etching the first insulation film and the second insulation film within the hole until the barrier film and the lower electrode are exposed, respectively;

forming a dielectric film over the cup-shaped lower electrode such that the dielectric film covers inner and outer peripheries and an inner bottom surface of the cup-shaped lower electrode, and then forming a second conductive film that covers the dielectric film, said dielectric film being made of a ferroelectric or high-dielectric-constant substance; and

patterning the dielectric film and the second conductive film simultaneously to thereby form a capacitor dielectric film and an upper electrode.

5. The method according to claim 4, wherein said barrier film is made of TiO_2 or Al_2O_3 or SiN.

6. The method according to claim 4, wherein the adhesion film comprises a Ti film or a TiO_2 film on the first insulation film.

7. The method according to claim 4, wherein the second conductive film is formed such that a gap defined between opposite surfaces of the dielectric film within the hole is filled with a part of the second conductive film.

9. The method according to claim 4, wherein a part of the upper electrode fills a gap defined between opposite surfaces of the dielectric film within the hole.

10. The method of claim 1, wherein the contact hole has the same cross sectional area in both the interlayer insulating film and the barrier film.

11. The method of claim 4, wherein the contact hole has the same cross sectional area in both the barrier film and the interlayer insulating film.

12. The method of claim 1, wherein the dielectric film covers each of an upper surface and all side surfaces of the protuberant lower electrode.